IN THE CLAIMS

Please amend claims 1-11 to read as follows:

1. (Amended) A method of restructuring a binary decision diagram representation of a hardware system, comprising acts of:

arranging variables of the binary decision diagram in a representation of a graph, corresponding to the hardware system, the graph having a top, nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, thereby to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions that depend on the variables labeling the one of the nodes;

traversing the graph from the top down to produce a list of labels in a selected order; and

using the list to restructure the binary decision diagram representation of the hardware system.

2. (Amended) An apparatus for restructuring a binary decision diagram representation of a hardware system, comprising :

a first storage circuit to store first bits representing variables of the binary decision diagram;

a second storage circuit; and

a processor, coupled to the first storage circuit and the second storage circuit, adapted to arrange the variables of the binary decision diagram in a representation of a graph having a top, nodes, and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes, the processor also being adapted to traverse the graph from the top down, and to output to the second storage circuit a list of labels in a selected order based upon traversal of the graph.

3. (Amended) A method of restructuring a binary decision diagram representative of a hardware system, the binary decision diagram including a plurality of variables, the method comprising acts of:

arranging variables of the binary decision diagram in a representation of a graph corresponding to the hardware system, the graph having a top, nodes, and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes;

traversing the graph from the top down to produce a list of the labels in a selected order;

sifting the variables based on the selected order; and

restructuring the binary decision diagram based on the act of sifting the variables.

4. (Amended) The method of claim 3, wherein the variables are sifted one-by-one to a deepest location.

5. The method of claim 3, wherein the variables are sifted one-by-one in the selected order to a deepest location followed by sifting in reverse order to a shallowest location.

6. (Amended) An apparatus for restructuring a binary decision diagram representative of a hardware system, comprising:

storage circuitry for storing bits representative of a set of functions as a binary decision diagram corresponding to the hardware system, the binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes; and

a processor adapted to detect a number of nodes of the binary decision diagram, and in response to the detection,

arranging the variables of the binary decision diagram on a graph having a top, nodes and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes,

traversing the graph from the top down, to produce a list of the labels in a selected order, and

sifting the variables of the binary decision diagram based on the selected order, wherein the sifted variables are written by the processors to the storage circuitry.

7. A method for proving the properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine variables of the internal signals, the method comprising acts of:

representing the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

substituting the functions which determine the variables of the internal signals;

arranging the variables of the binary decision diagram on a graph having a top, nodes and leaves, the nodes being labeled with the variables of the system and the leaves being labeled with a set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes;

traversing the graph from the top down to produce a list of the labels in a selected order; and

sifting the variables of the binary decision diagram based on the selected order.

8. (Amended) An apparatus for proving properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine values of the internal signals, the apparatus comprising:

storage circuitry for storing bits representative of a set of functions which represent the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

a processor that substitutes the functions which determine the values of the internal signals into the set of functions representing the system and detects an increase in a number of the nodes of the binary decision diagram, and in response to the detection, arranges the variables of the binary decision diagram on a graph having a top, nodes and leaves, the nodes being labeled with a set of functions to generate labels for the nodes and leaves, whereby the set of